

PHD/PHP36N03LT

N-channel TrenchMOS logic level FET

Rev. 02 — 8 June 2006

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Logic level compatible
- Low gate charge

1.3 Applications

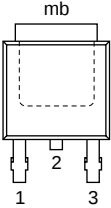
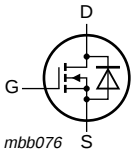
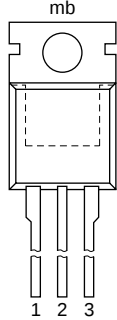
- DC-to-DC converters
- Switched-mode power supplies

1.4 Quick reference data

- $V_{DS} \leq 30 \text{ V}$
- $I_D \leq 43.4 \text{ A}$
- $R_{DS(on)} \leq 17 \text{ m}\Omega$
- $P_{tot} \leq 57.6 \text{ W}$

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	drain (D) [1]		
3	source (S)		
mb	mounting base; connected to drain		
			
		SOT428 (DPAK)	SOT78 (3-lead TO-220AB)

[1] It is not possible to make a connection to pin 2 of the SOT428 package.

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3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PHD36N03LT	DPAK	plastic single-ended surface-mounted package; 3 leads (one lead cropped)	SOT428
PHP36N03LT	SC-46	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

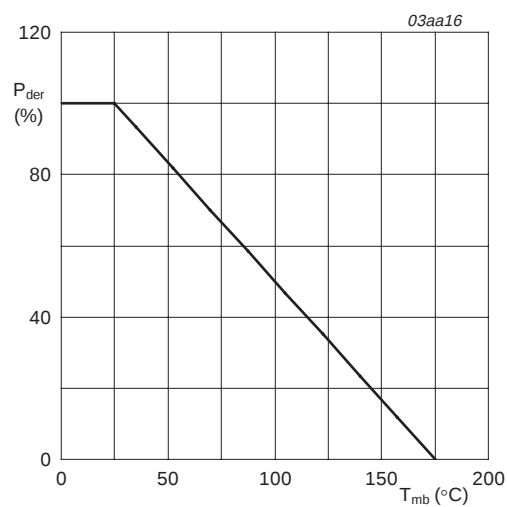
Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2 and 3	-	43.4	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 2	-	30.7	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	173.6	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 1	-	57.6	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C

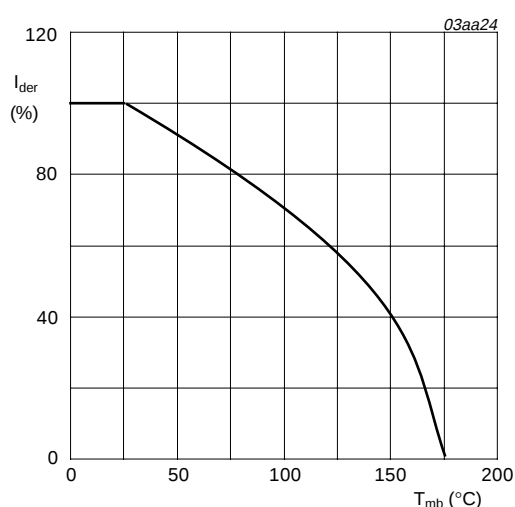
Source-drain diode

I_S	source current	$T_{mb} = 25\text{ °C}$	-	43.4	A
I_{SM}	peak source current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	173.6	A



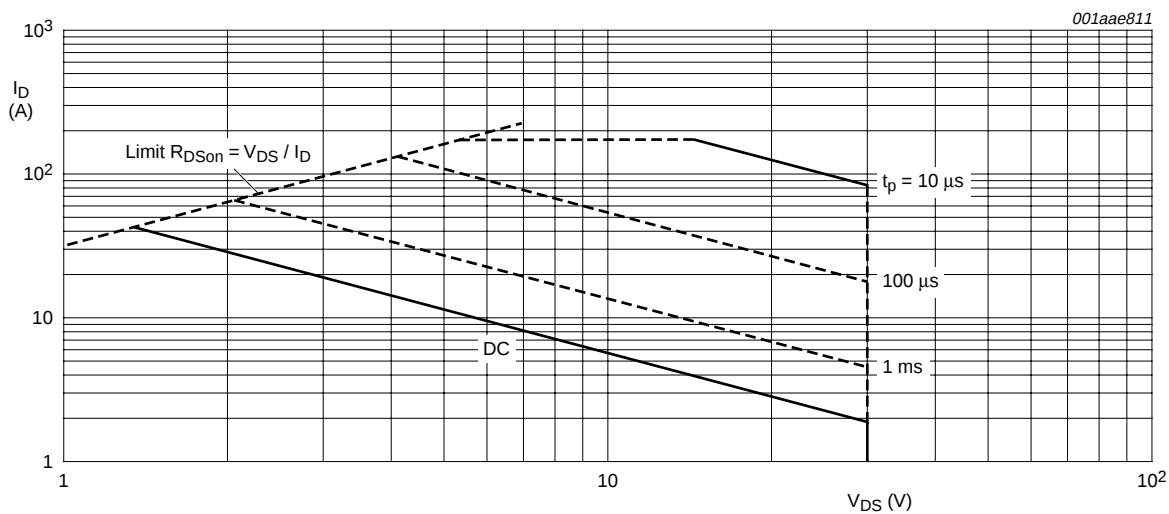
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 10 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in free air	-	60	-	K/W
	SOT428	minimum footprint	[1] -	75	-	K/W
	SOT404 minimum footprint	[1] -	-	50	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

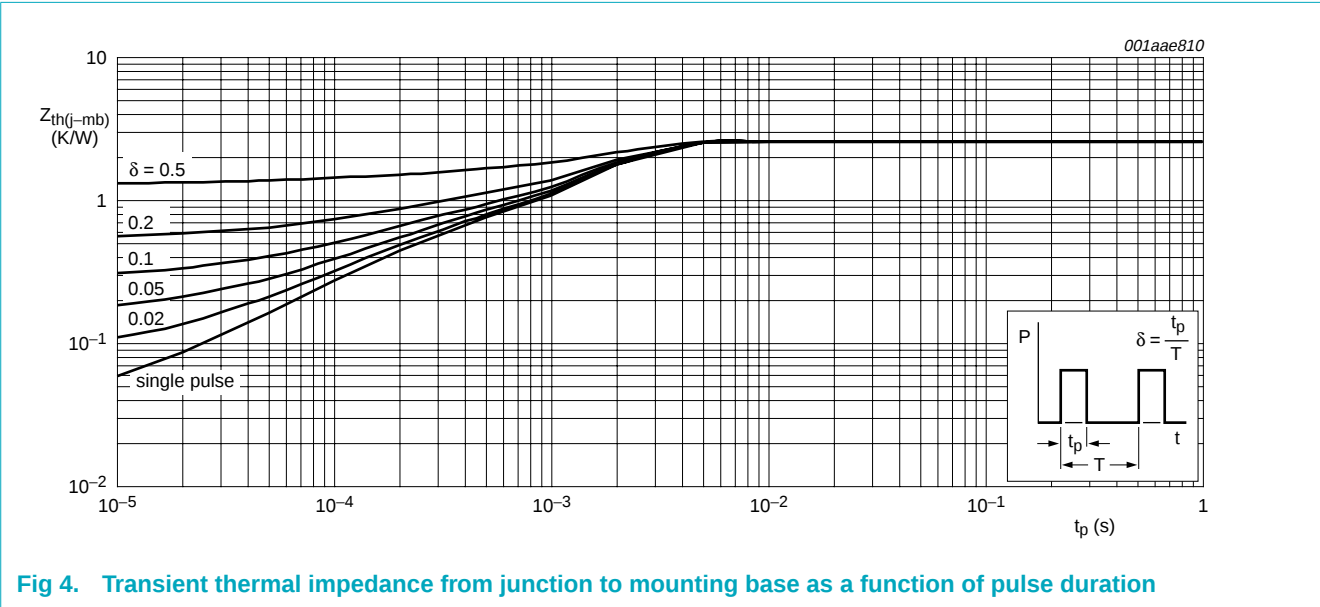


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5. Characteristics

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	30	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{DS} = V_{GS}$; see Figure 9 and 10				
		$T_j = 25\text{ }^{\circ}\text{C}$	1	1.5	2	V
		$T_j = 175\text{ }^{\circ}\text{C}$	0.5	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	-	-	2.2	V
I_{DSS}	drain leakage current	$V_{DS} = 24\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	0.05	1	μA
		$T_j = 175\text{ }^{\circ}\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 12\text{ A}$; see Figure 6 and 8				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	18	22	m Ω
		$T_j = 175\text{ }^{\circ}\text{C}$	-	32.4	39.6	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; see Figure 6 and 8	-	14	17	m Ω
		$V_{GS} = 3.5\text{ V}$; $I_D = 5.2\text{ A}$; see Figure 6 and 8	-	22	40	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 36\text{ A}$; $V_{DS} = 15\text{ V}$; $V_{GS} = 10\text{ V}$; see Figure 11 and 12	-	18.5	-	nC
Q_{GS}	gate-source charge		-	4.2	-	nC
Q_{GD}	gate-drain charge		-	2.9	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; see Figure 14	-	690	-	pF
C_{oss}	output capacitance		-	160	-	pF
C_{rss}	reverse transfer capacitance		-	110	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}$; $R_L = 0.6\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_G = 10\text{ }\Omega$	-	6	-	ns
t_r	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	33	-	ns
t_f	fall time		-	19	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; see Figure 13	-	0.97	1.2	V

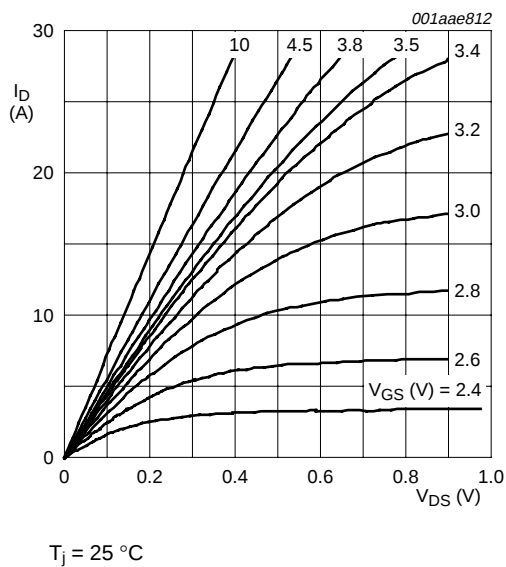


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

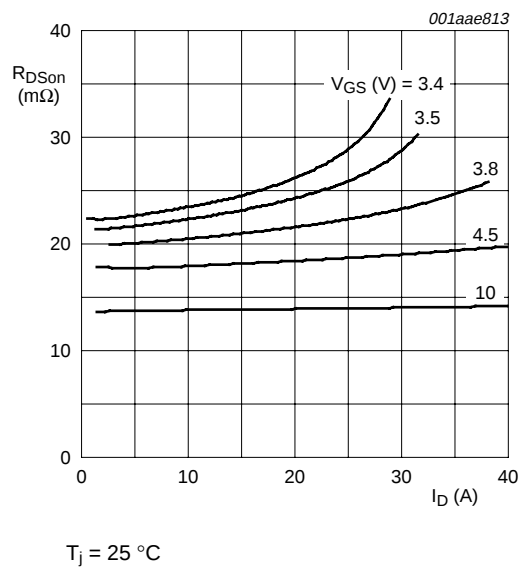


Fig 6. Drain-source on-state resistance as a function of drain current; typical values

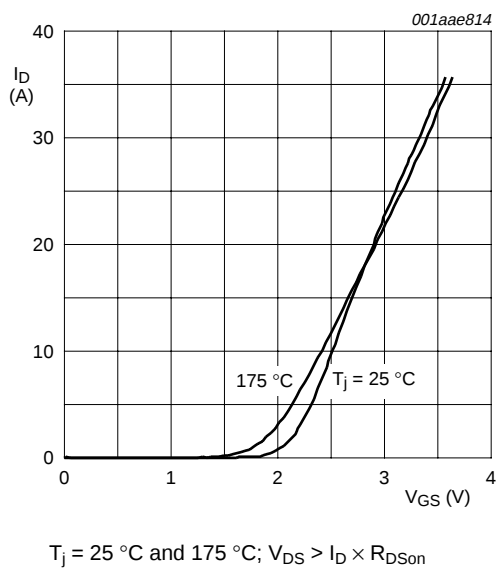


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

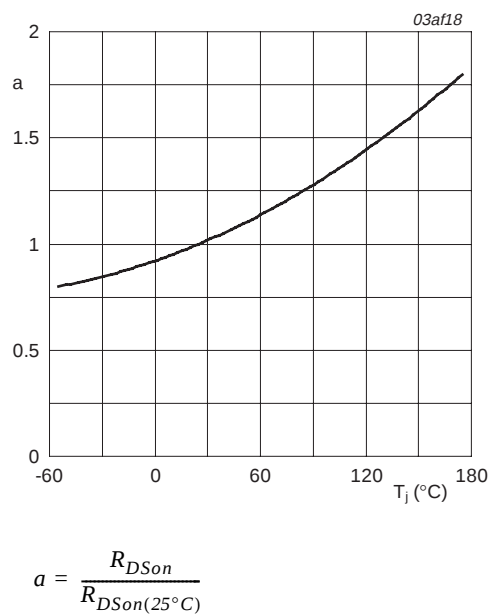
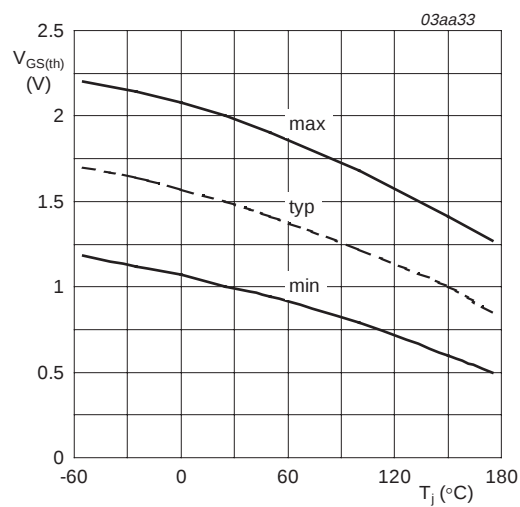
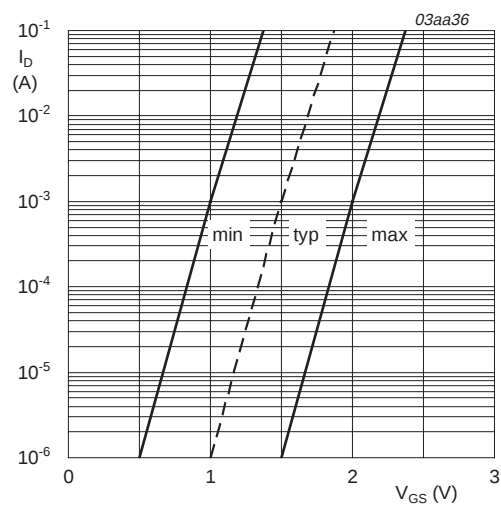


Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



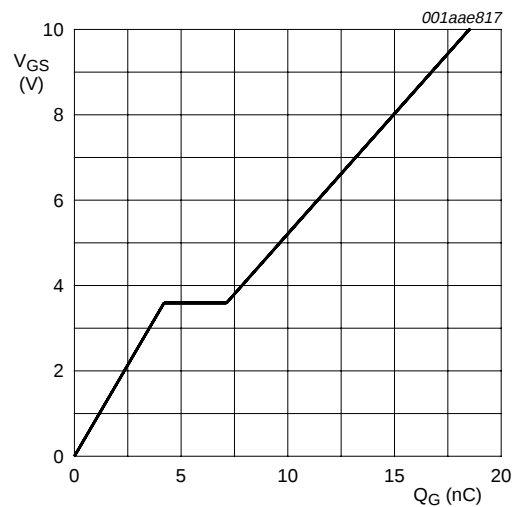
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ °C}$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 36 \text{ A}$; $V_{DS} = 15 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

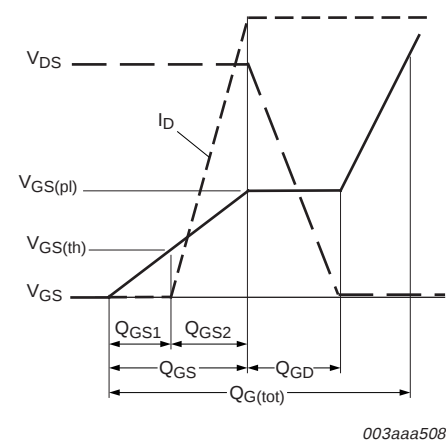
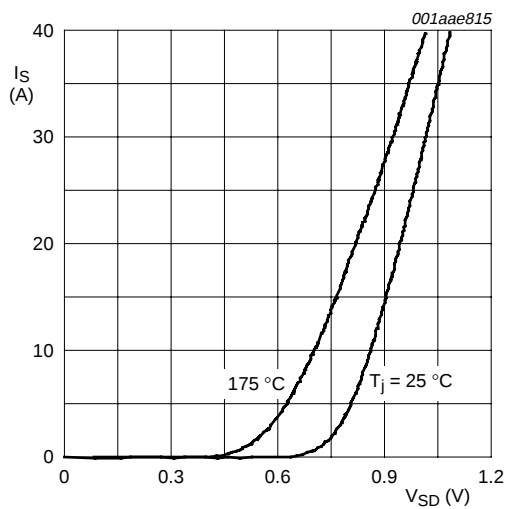
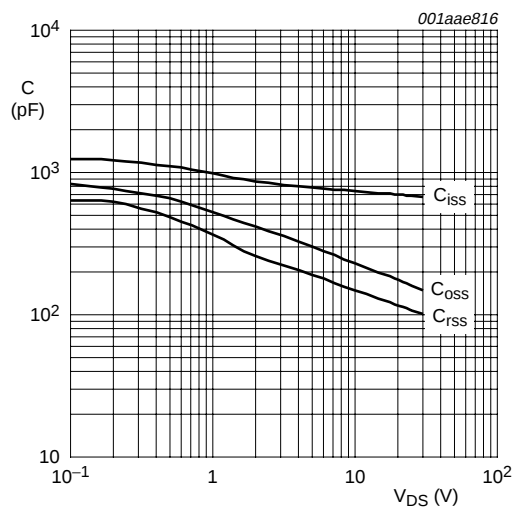


Fig 12. Gate charge waveform definitions



$T_J = 25\text{ °C}$ and 175 °C ; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

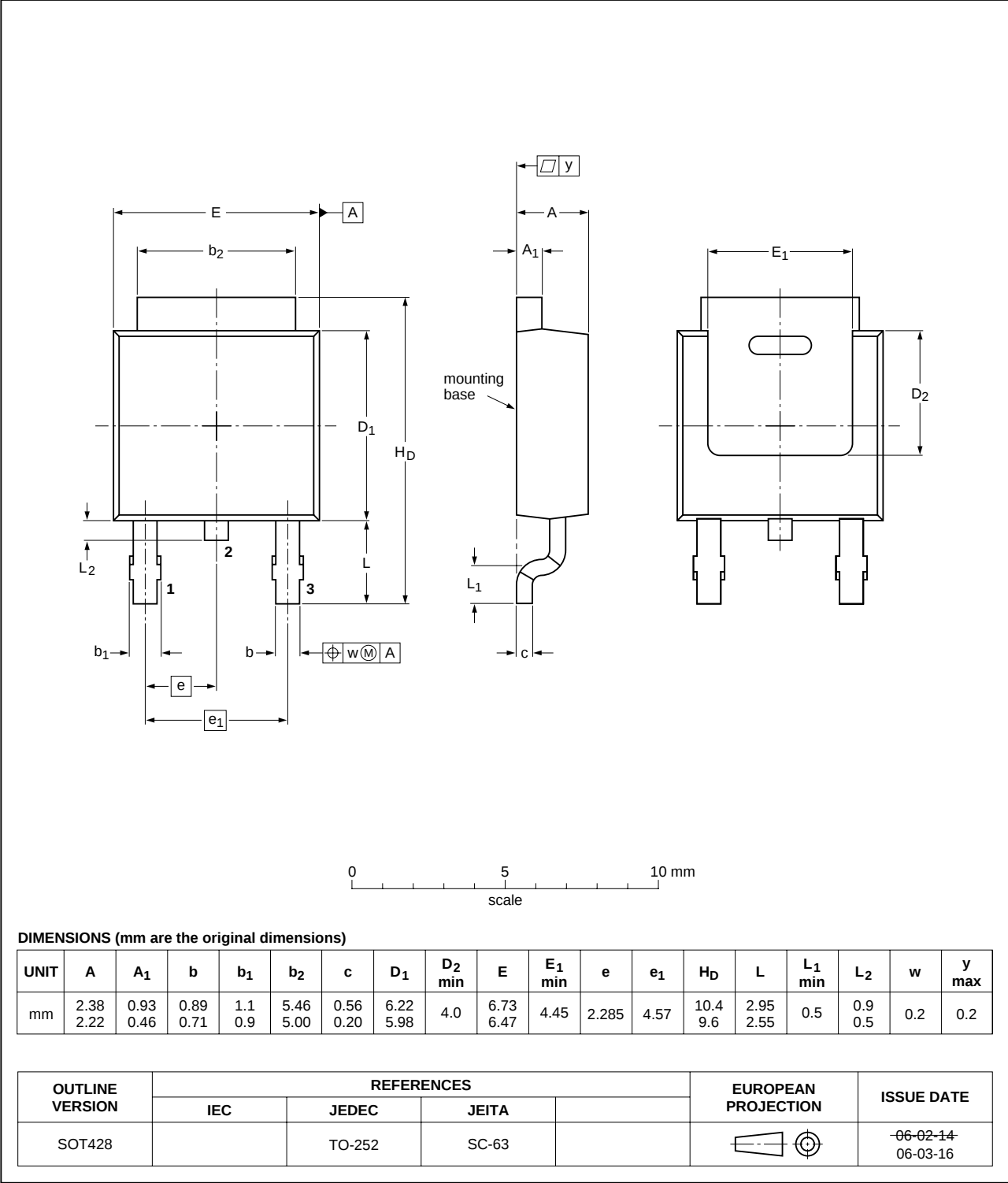


Fig 15. Package outline SOT428 (DPAK)

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

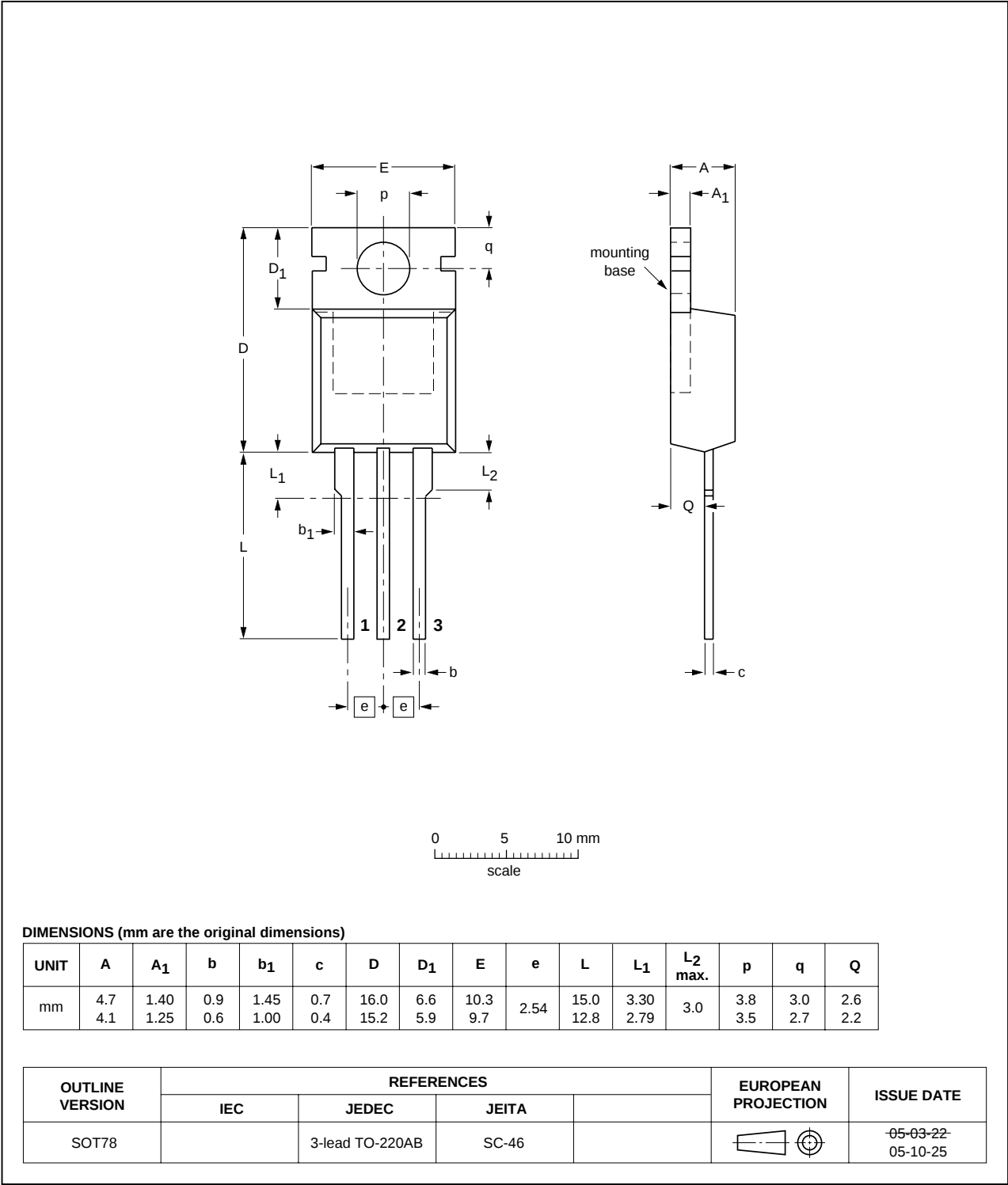


Fig 16. Package outline SOT78 (3-lead TO-220AB)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD_PHP36N03LT_2	20060608	Product data sheet	-	PHD36N03LT-01
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Addition of PHP36N03LT			
PHD36N03LT-01 (9397 750 11613)	20030630	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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